Amendments to the Specification:

Please amend the paragraph beginning on page 9, line 25, as follows:

The CE#, WE#, and OE# signals are also provided to input/output (I/O) logic 412 which, in response to these signals indicating a read or write command, enables a data input buffer 416 and an data output buffer 418, respectively. The I/O logic 412 also provides signals to an address input buffer 422 in order for address signals to be latched by an address latch 424. The latched address signals are in turn provided by the address latch 424 to an address multiplexer 428 under the command of the WSM 406. The address multiplexer 428 selects between the address signals provided by the address latch 424 and those provided by an address counter 432. The address signals provided by the address multiplexer 428 are used by the address decoders 440a, 440b to access the memory cells of memory banks 444a, 444b that correspond to the address signals. Based on the decoded address, row activation signals are provided to the appropriate row drivers 500 to drive the respective word lines for accessing the memory cells. A gating/sensing circuit 448a, 448b is coupled to each memory bank 444a, 444b for the purpose of programming and erase operations, as well as for read operations. An automatic power saving (APS) control circuit 449 receives address signals from the address input buffer 422 and also monitors the control signals RP#, CE#, OE#, and WE#. When none of these lines toggle within a time-out period, the APS control circuit 449 generates control signals to place the gating/sensing circuits 448a, 448b in a power saving mode of operation.

Please amend the paragraph beginning on page 10, line 13, as follows:

During a read operation, data is sensed by the gating/sensing circuit 448a, 448b and amplified to sufficient voltage levels before being provided to an output multiplexer 450. The read operation is completed when the WSM 406 instructs an output buffer 418 to latch data provided from the output multiplexer 450 to be provided to the external processor. The output multiplexer 450 can also select data from the ID and status registers 408, 410 to be provided to the output buffer 418 when instructed to do so by the WSM 406. During a program or erase operation, the I/O logic 412 commands the data input buffer 416 to provide the data signals to a

data register 460 to be latched. The WSM 406 also issues commands to program/erase circuitry 464 which uses the address decoder 440 to carry out the process of injecting or removing electrons from the memory cells of the memory banks 444a, 444b to store the data provided by the data register 460 to the gating sensing circuit 448. ~~The program/erase circuitry 464 also provides the erase voltages VPP and VPP to the discharge controller 300. The discharge controller 300 operates as previously described in response to the DIS1 and DIS2 signals from the WSM 406 to discharge the array source AS, p-well drive, PWDRV, and word lines WL in a selected block of memory cells in the memory banks 444a, 444b.~~ To ensure that sufficient programming or erasing has been performed, a data comparator 470 is instructed by the WSM 406 to compare or verify the state of the programmed or erased memory cells to the data latched by the data register 460. During all of these modes of operation the CSM 404 maintains the PSM signal inactive so that the row drivers 500 operate in the normal mode as previously described.